

A CMOS Image Sensor Pixel Readout Circuit Design Using Back-End-of-Line (BEOL)-Compatible Oxide Transistors

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Abstract—This paper presents a novel pixel readout circuit designed for a $0.56\text{ }\mu\text{m}$ pixel pitch CMOS image sensor, with back-end-of-line (BEOL)-compatible amorphous oxide semiconductor channel transistors. By monolithically stacking W-doped In_2O_3 (IWO) transistors onto two BEOL tiers above each photodiode, the proposed voltage-domain global shutter architecture preserves transistor area for improved noise performance without increasing the complexity associated with additional wafer stacking. Measured low-frequency ($1/f$) noise characteristics of the IWO transistor reveal a Hooge's parameter ($\alpha_H \approx 4.98 \times 10^{-3}$) comparable to conventional silicon MOSFETs with high- k gate dielectrics. Noise analysis and circuit simulation results demonstrate a read noise of 1.81 e^- and a dynamic range of 70.4 dB , highlighting the potential of BEOL-stacked oxide semiconductor devices for next-generation submicron CMOS image sensors.

Index Terms—CMOS image sensor, IWO transistor, back-end-of-line, pixel readout circuit, low noise, global shutter.

I. INTRODUCTION

CMOS image sensors (CIS) have been rapidly scaled to meet the rising demand for higher resolutions, with $0.56\text{ }\mu\text{m}$ pixel pitches now defining the cutting edge in sensor miniaturization [1] [2] [3]. This submicron scaling is highly desirable for packing more pixels onto the same die area, thereby enhancing image quality and enabling higher-resolution devices. However, meeting these miniaturization goals poses significant challenges. The full well capacity (FWC) reduces as the photodiode area decreases. Moreover, the smaller transistor footprint limits the source follower (SF) design space, restricting dynamic range under low-light conditions and making the SF transistor more susceptible to flicker noise and random telegraph signals (RTS) [1].

CMOS image sensors employ several strategies to navigate through the submicron photodiode pitch region, by leveraging advanced packaging techniques such as wafer stacking with hybrid bonding. Fig. 1 illustrates various wafer stacking schemes currently utilized in state-of-the-art CMOS image sensors. One critical issue when scaling pixels below $1\text{ }\mu\text{m}$ pitch is managing flicker noise originating from the source follower (SF) transistor, as random telegraph signals and temporal noise are inversely proportional to the transistor area [1]. As depicted in Fig. 1(a), a conventional two-wafer stacking scheme integrates pixel and logic wafers, but positions the pixel readout circuitry laterally at the periphery of each back-illuminated photodiode, restricting the available space for

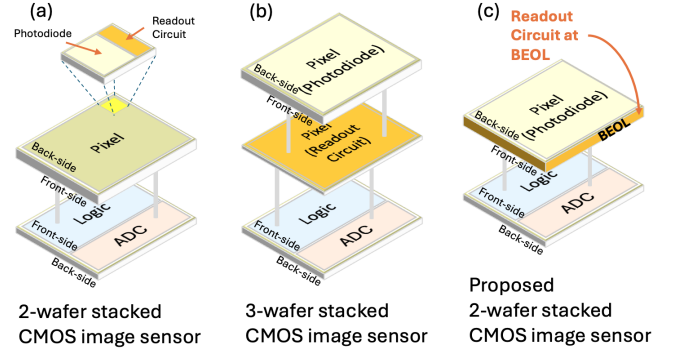


Fig. 1. An illustration of the (a) conventional 2-wafer stacked CMOS image sensor with photodiode and readout circuit on the same pixel wafer. (b) 3-wafer stacked CMOS image sensor with separate wafers for photodiode, readout circuit, and logic (image signal processor, etc.) / ADC [6]. (c) Proposed 2-wafer stacked CMOS image sensor, stacking the readout circuit in the BEOL of the pixel wafer.

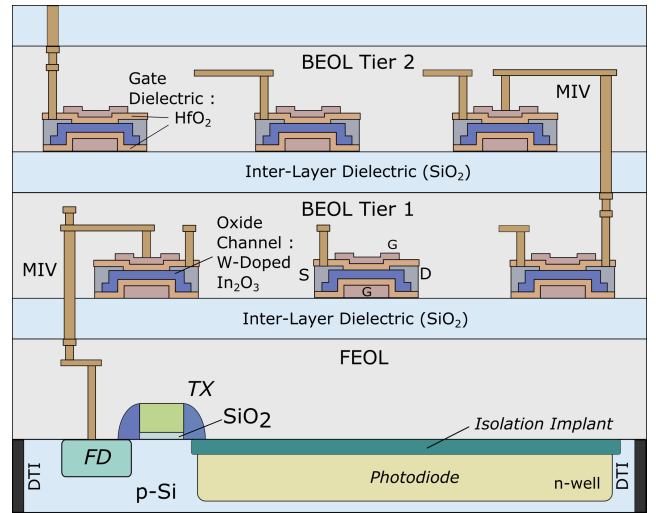


Fig. 2. An illustration of the device structure of a double-gated IWO transistor in proposed organization of photodiode, FD node, FEOL/BEOL devices and routing in a single pixel.

the SF transistor. To alleviate this limitation, recent efforts have adopted a three-wafer stacking approach (Fig. 1(b)), in which dedicated wafers are individually allocated for the photodiode, pixel readout transistors, and logic circuits (e.g.,

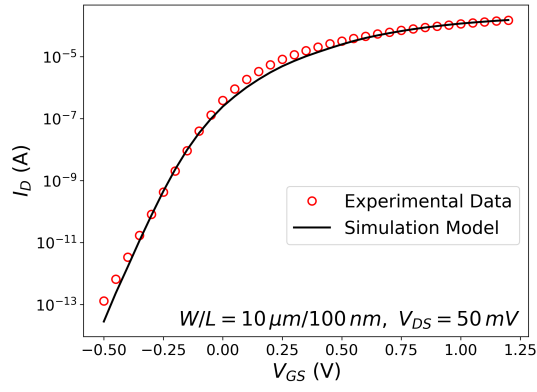


Fig. 3. Log-scale $I_D - V_{GS}$ curve of the IWO transistor. Curves generated by a compact model validated with experimental data reported in [14].

image signal processing, ADC) by rearranging readout circuitry elements [8] [9] [16]. By maintaining a large area for the SF transistor, this wafer stacking approach enables higher pixel counts and improved noise performance by isolating different functions onto distinct layers, as demonstrated in recent high-resolution CMOS image sensor developments [10]. In addition, pixels sharing a readout circuit along with switchable conversion gain provide a higher FWC for a wider dynamic range with increased conversion gain. Furthermore, vertical transfer gates and high-aspect-ratio deep trench isolation (DTI) provide additional room for a higher signal-to-noise ratio [5].

Building on these strategies, we propose an alternative approach that leverages back-end-of-line (BEOL)-compatible transistor technology, which can be monolithically stacked above the photodiode without additional wafer layers. One promising candidate is amorphous oxide semiconductor channel transistors that could be fabricated under the BEOL thermal budget ($<400^\circ\text{C}$), specifically, W-doped In_2O_3 (IWO) transistors. The tungsten in the IWO material acts as both an electron donor and a stabilizer by modulating the trapping and detrapping events of oxide channel carriers. Compared to other oxide channel transistors, IWO devices exhibit low leakage currents ($<10^{-15} - 10^{-18} \mu\text{A}/\mu\text{m}$) [11], a high $I_{\text{on}}/I_{\text{off}}$ ratio ($>4 \times 10^9$) and moderate electron mobility ($\sim 10 - 20 \text{ cm}^2/\text{V}\cdot\text{s}$) [12]. Additionally, IWO transistors demonstrate excellent low-frequency ($1/f$) noise behavior, making them particularly suitable for pixel readout circuits, where flicker noise significantly affects the sensor's overall noise performance [13]. The device structure of a dual-gated IWO transistor is shown in Fig. 2. The logarithmic $I_d - V_g$ curves of the IWO transistor shown in Fig. 3 are generated by a compact model validated with experimental data reported in [14].

In this work, we design and simulate a voltage-domain global shutter pixel architecture leveraging two tiers of IWO transistors stacked above the photodiode. We analyze the low-frequency noise characteristics of these oxide transistors and apply these findings to estimate pixel-level read noise. Circuit simulations demonstrate a read noise of 1.81 e^- and a dynamic range of 70.4 dB, with power consumption comparable to

conventional silicon-based readout circuits. The significance of this approach is two-fold. First, by stacking transistors monolithically within the BEOL layers of the same wafer as in Fig. 1(c), we reduce the fabrication complexity and associated cost compared to three-wafer stacking approach. Second, the noise and dynamic range performance achieved with these IWO transistors highlights strong potential for further scaling toward next-generation submicron CMOS image sensors. This paper details the proposed pixel readout circuit, discusses IWO transistor characterization, and examines the resulting noise and dynamic range, thereby demonstrating a promising route for future miniaturized CMOS image sensor designs.

II. PROPOSED PIXEL ARCHITECTURE AND LAYOUT

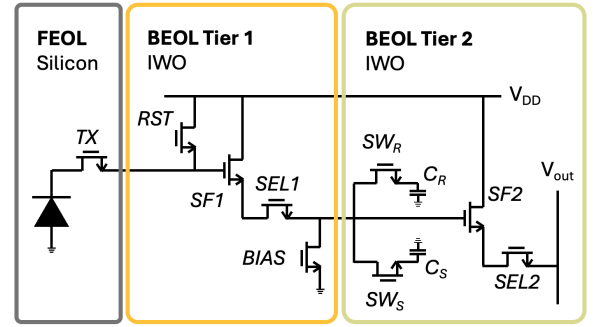


Fig. 4. Circuit Schematic of voltage-domain global shutter pixel.

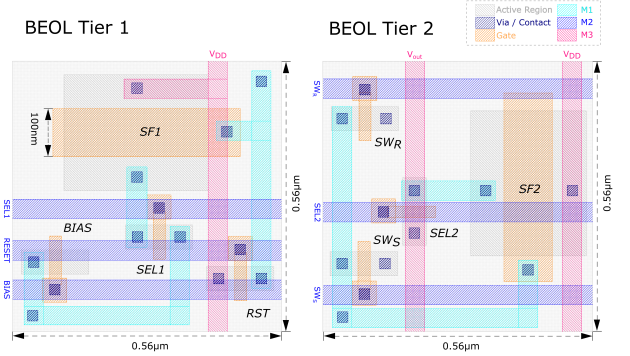


Fig. 5. Layout of proposed pixel readout circuit in BEOL tier 1 and tier 2.

A circuit schematic of the backside-illuminated (BSI) voltage-domain global shutter pixel is shown in Fig. 4. To maximize transistor area, particularly for the source follower (SF), the pixel readout circuit is vertically arranged into two monolithic back-end-of-line (BEOL) tiers positioned directly above the photodiode (PD) and transfer gate (TX). Both BEOL tiers, including all associated readout transistors and correlated double sampling (CDS) circuitry, are stacked within the compact pixel footprint of $0.56 \times 0.56 \mu\text{m}^2$. On the front-end-of-line (FEOL) level, the TX transistor connects the PD to the floating diffusion (FD) node. The FD node is vertically connected through a monolithic interlayer via (MIV) to the first BEOL tier, which includes the reset transistor (RST), the

primary source follower transistor (SF1), a select transistor (SEL1), and a bias transistor (BIAS). The second (upper) BEOL tier implements CDS functionality and contains a second source follower transistor (SF2), a row select transistor (SEL2), and two switch transistors (SW_R and SW_S) for storing reset and signal voltages onto three-dimensional (3D) metal-insulator-metal (MIM) capacitors, which are also connected via MIVs. This vertical integration strategy effectively addresses the stringent area constraints associated with a $0.56 \times 0.56 \mu\text{m}^2$ pixel footprint.

Fig. 5 shows the layout of the proposed two-tier pixel readout circuit. The two SF transistors are designed with channel dimensions of 300 nm width by 100 nm length to achieve low-noise performance, while the other IWO transistors have more compact dimensions of 50 nm width by 25 nm length. Metal interconnections within each tier use a metal pitch of 40 nm (M1-M3), and inter-tier MIV connections have a diameter of 30 nm [15].

III. IWO TRANSISTOR NOISE CHARACTERIZATION

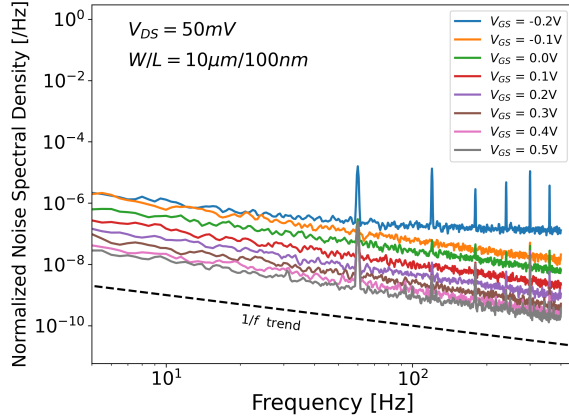


Fig. 6. Normalized noise power spectrum of the IWO transistor ($W/L = 10 \mu\text{m}/100 \text{nm}$) at $V_{DS} = 50 \text{mV}$.

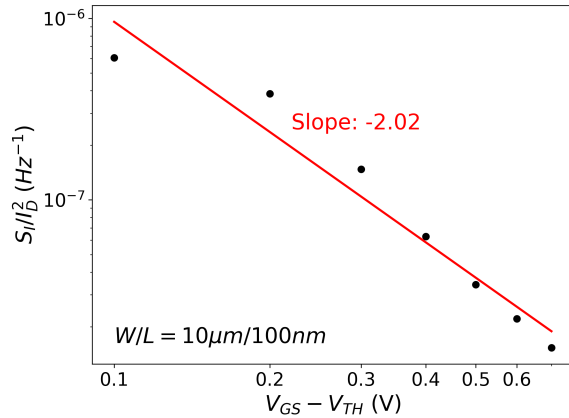


Fig. 7. Normalized drain-current noise spectral density of the IWO transistor ($W/L = 10 \mu\text{m}/100 \text{nm}$) at various V_{GS} , showing an inverse square dependence on the overdrive voltage.

Fig. 6 shows the measured frequency dependence of the normalized drain-current noise spectral density (S_{I_d}/I_d^2) of the IWO transistor ($W/L = 10 \mu\text{m}/100 \text{nm}$) at different gate-source voltages (V_{GS}) [13]. The drain-current noise power spectral density (S_{I_d}) follows a $1/f$ trend, confirming that flicker noise is the dominant low-frequency noise component in these transistors [13]. This behavior is consistent with the McWhorter model [19], where $1/f$ noise primarily arises from random trapping and detrapping of carriers at the semiconductor-oxide (IWO/ HfO_2) interface.

Fig. 7 further illustrates the normalized noise spectral density (S_{I_d}/I_d^2) as a function of overdrive voltage ($V_{GS} - V_{th}$) at $f = 10 \text{Hz}$. The observed inverse square dependence on the overdrive voltage confirms the carrier number fluctuation mechanism described by McWhorter's theory. Within this framework, the normalized current noise power spectral density can be expressed as:

$$\frac{S_{I_d}}{I_d^2} = \frac{k^*}{f} \frac{2}{C_{ox}^2 W L} \frac{1}{(V_{GS} - V_{th})^2}, \quad (1)$$

where k^* is a fitting parameter related to interface trap densities and tunneling probabilities, f is the frequency, I_d is the drain current, C_{ox} is the oxide capacitance per unit area, W and L represent the transistor channel width and length, respectively, and V_{GS} and V_{th} denote the gate-to-source and threshold voltages.

Using the measured noise data, we extracted Hooge's parameter (α_H), a commonly used figure-of-merit for comparing noise levels across different semiconductor materials and devices. Hooge's parameter is given by:

$$\alpha_H = \left(\frac{S_{I_d}}{I_d^2} \right) \frac{C_{ox} W L f}{q} (V_{GS} - V_{th}), \quad (2)$$

where q is the electron charge. Using an oxide capacitance per unit area of $C_{ox} = 2.25 \times 10^{-4} \text{F m}^{-2}$, we extracted an average $\alpha_H \approx 4.98 \times 10^{-3}$, which is comparable to conventional silicon MOSFET devices with high- k gate dielectrics [18]. This result highlights the suitability of IWO transistors as a candidate for low-noise, space-efficient pixel readout circuitry.

IV. PIXEL READOUT PERFORMANCE

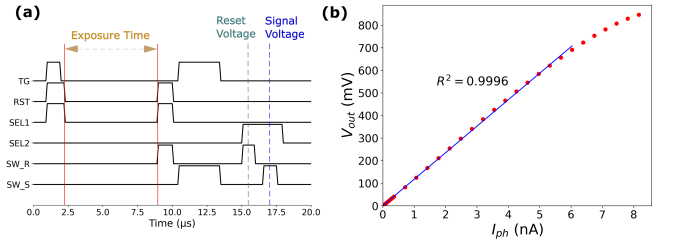


Fig. 8. (a) Timing diagram of the proposed pixel and the (b) V_{out} vs I_{ph} curve.

To verify how the measured noise performance of the IWO transistor translates into pixel-level results, we performed circuit-level simulations of our proposed two-tier pixel architecture. First, the voltage gain (A_v) of the source follower (SF)

TABLE I
COMPARISON OF VARIOUS PIXEL ARCHITECTURES

Parameter	This Work	Samsung ISSCC 2024 [1]	Samsung IISW 2023 [2]	OmniVision IISW 2023 [4]	Samsung VLSI 2022 [7]	Samsung IEDM 2022 [8]	OmniVision IS&T 2023 [16]
Pixel Pitch (μm)	0.56	0.56	0.56	0.56	0.60	1.8	2.2
Device Structure	2 wafer + BEOL	2 wafer	2 wafer	2 wafer	2 wafer	3 wafer	3 wafer
FWC (e^-)	6,000	3,700/59,000	4,700	5,500/72,000	6,000	14,000	12,000
Read Noise (e^-)	1.81	1.6	1.6/2.3	20.2	1.5	1.8	3.1
Dynamic Range (dB)	70.4	91.3	73	71	72	-	-

transistor was characterized by simulating the output voltage as a function of the input voltage. The simulated voltage gain (A_v) is approximately 0.85 within the voltage range of the floating diffusion (FD) node at a supply voltage (V_{DD}) of 2.5 V.

We then conducted pixel-level noise analysis informed by the characterized low-frequency ($1/f$) noise properties of the IWO transistor. The simulated pixel output noise is dominated by low-frequency components, resulting in a noise voltage of $87.857 \mu\text{V}_{\text{rms}}$. By setting the FD node capacitance to match a full well capacity (FWC) of 6,000 electrons, representative of a $0.56 \mu\text{m}$ pixel pitch photodiode, we obtained a conversion gain of $49.7 \mu\text{V}/e^-$. This yields an estimated pixel read noise of $1.81 e^-$ and a dynamic range of 70.4 dB.

Fig. 8 (a) shows the simulated timing diagram for a single readout cycle, and Fig. 8 (b) illustrates the corresponding pixel output voltage as a function of photocurrent generated by an analytical photodiode model. The power consumption of the proposed pixel readout circuit is approximately 96.95 nW per pixel during a combined exposure and readout period of $20 \mu\text{s}$ at a 2.5 V supply, translating to about $49.6 \mu\text{W}$ per column (assuming 512 pixels per column). For comparison, we simulated an identical pixel circuit configuration with all IWO transistors replaced by conventional silicon MOSFETs (using the FreePDK [17]), resulting in a slightly lower power consumption of 89.89 nW per pixel. Our BEOL-stacked IWO transistor implementation thus represents a moderate power overhead of about 7.9%, highlighting its practicality.

Table I summarizes key performance parameters—including pixel pitch, full well capacity (FWC), read noise, and dynamic range—for our proposed pixel architecture alongside recent pixel designs reported in the literature. Compared with previously reported $0.56 \mu\text{m}$ pixel architectures [1], [2], [4], our design achieves a balance between read noise ($1.81 e^-$) and dynamic range (70.4 dB). Although designs featuring dual conversion gain [1], [4] achieve substantially higher maximum FWC and wider dynamic ranges by employing shared readout circuits, our single conversion gain pixel, which dedicates one readout circuit per pixel, exhibits significantly lower read noise than some reported pixels of comparable dimensions [4]. These results illustrate that the monolithic BEOL-stacked IWO transistor approach effectively balances pixel complexity, noise, and dynamic range, demonstrating its potential as a

practical and efficient technology solution for next-generation submicron CMOS image sensors.

V. CONCLUSION

In this paper, we proposed a novel pixel readout circuit architecture utilizing monolithically stacked BEOL-compatible oxide transistors to address the critical challenges associated with submicron pixel scaling. Our design integrates two tiers of W-doped In_2O_3 (IWO) transistors directly above the photodiode, preserving transistor dimensions crucial for achieving low-noise performance. The IWO transistors were carefully characterized, exhibiting low-frequency ($1/f$) noise behavior comparable to conventional silicon MOSFETs, leading to a simulated pixel-level read noise of $1.81 e^-$ and a dynamic range of 70.4 dB. Our findings indicate that BEOL-compatible oxide transistors offer a practical approach to overcoming area constraints and source follower transistor noise issues in advanced pixel designs, paving the way for future high-resolution, low-noise CMOS image sensors.

ACKNOWLEDGMENT

This work is in part supported by NSF-2415330 and was supported by the National NanoFab Center (NNFC) grant funded by the Korea government (MSIT) (No. RS-2024-00440244). The authors would also like to thank Prof. Tae-Hyeon Kim of Seoul National University of Science and Technology for his valuable collaboration and support.

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